Remarks

The non-final Office Action dated May 23, 2008 lists the following rejection: claims 1-5 stand rejected under 35 U.S.C. § 103(a) over Itoh *et al.* under 35 U.S.C. § 103(a) (U.S. Patent No. 5,430,397) in view of Hiiragizawa (U. S. Patent No. 5,963,075). In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in the instant Office Action unless Applicant expressly indicates otherwise.

Applicant respectfully traverses the § 103(a) rejection of claims 1-5 because, among other reasons, the modification of the Itoh reference proposed by the Office Action would render Itoh unsatisfactory for its intended purpose. According to M.P.E.P. § 2143.01, if a "proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification". *See, also, In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984). The Office Action proposes to modify Itoh such that the clock signals provided by one of the clock distribution circuits 6a-f of blocks 2a-f are phase shifted relative to the clock signals provided by another one of the clock distribution circuits 6a-f of the blocks 2a-f. *See, e.g.,* Figures 2-4. A stated purpose of the Itoh reference, however, is to provide a clock distribution circuit for an LST chip that can make available clock signals with the least skew to every part of the chip (*i.e.,* to make the clock signals provided to every part of the chip in phase with each other). *See, e.g.,* Col. 4:15-27 and Col. 9:59 to Col. 10:9. Applicant submits that the Office Action's proposed modification would shift the phase of the clock signals of one of blocks 2a-f relative to the phase of the clock signals of another one of blocks 2a-f, thus rendering Itoh unsatisfactory for its intended purpose of having the clock signals be in phase with each other. As such, there would be no motivation for the skilled artisan to modify Itoh in the manner proposed by the Office Action. Accordingly, the § 103(a) rejection of claims 1-5 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 1-5 because the cited combination does not correspond to the claimed invention. Applicant maintains that the cited portions of the Hiiragizawa reference do not teach or suggest aspects of the claimed invention directed to a set of synchronized local clock signals of a first block being phase

shifted relative to a set of synchronized local clock signals of a second block. In the Response dated January 17, 2008, Applicant explained in detail that the cited portions of Hiiragizawa do not correspond to these aspects of the claimed invention. The rejection presented in the instant Office Action continues to rely upon the same teaching of Hiiragizawa without responding to the substance of Applicant's previous arguments as required. *See, e.g.,* M.P.E.P. § 707.07(f) ("Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it."). Applicant submits that, since the rejection in the instant Office Action continues to rely upon the same teachings of the Hiiragizawa reference, the Examiner should have responded in substance to Applicant's previous arguments regarding the lack of correspondence being these portions of Hiiragizawa and the claimed invention. The following discussion particularly addresses the lack of correspondence between the cited portions of Hiiragizawa and the claimed invention.

The Office Action acknowledges that the Itoh reference does not disclose that a set of synchronized local clock signals of a first block are phase shifted relative to a set of synchronized local clock signals of a second block as in the claimed invention. The Office Action then cites to portions of Hiiragizawa that teach a single clock signal M 111 that is provided to peripheral block A 104 and a single clock signal N 112 that is provided to peripheral block B 105, with clock signal M 111 being out of phase with clock signal N 112. *See, e.g.,* Figures 5 and 7. Thus, the cited portions of Hiiragizawa only teach that two clock signals are out of phase with each other. These portions of Hiiragizawa do not teach that a set of synchronized local clock signals of a first block are phase shifted relative to a set of synchronized local clock signals of a second block as in the claimed invention. As such, the Office Action fails to cite to any reference that teaches such aspects of the claimed invention. As Applicant's disclosure is the only reference present that teaches these aspects of the claimed invention, Applicant submits that any combination that includes such aspects would appear to be based upon improper hindsight reconstruction using Applicant's disclosure as a template. *See, e.g.,* M.P.E.P. § 2142. Accordingly, the § 103(a) rejection of claims 1-5 is improper and Applicant request that it be withdrawn. Should any rejection based on the above discussed teachings of the Hiiragizawa reference be maintained, Applicant requests clarification

regarding the basis for the continued reliance upon Hiiragizawa in view of its lack of correspondence to the claimed invention.

Applicant further traverses the § 103(a) rejection of claim 2 because the Office Action fails to provide any reason why the skilled artisan would modify the Itoh reference. This approach is contrary to the requirements of § 103 and relevant law. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007)

> Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

The Office Action proposes to combine Hiiragizawa's address/signal bus 106 with the Itoh reference; however, the Office Action fails to provide any reason why the skilled artisan would combine these teachings. Moreover, it is unclear to Applicant how the Office Action is asserting that Hiiragizawa's address/signal bus 106 is a one-way data path. For example, Hiiragizawa teaches that the interface circuit of block 104 uses address/signal bus 106 for two-way communication. *See, e.g.,* Figure 8 and Col. 7:5-30. Applicant notes that the Office Action even asserts that address/signal bus 106 is a two-way data bus in relation to the rejection of claim 5. *See, e.g.,* page 4 of the instant Office Action. Accordingly, the § 103(a) rejection of claim 2 is improper and Applicant requests that it be withdrawn.

Applicant has added new claims 6-10, which depend from claim 1. Applicant submits that claims 6-10 are allowable over the cited references for at least the reasons discussed above in relation to the impropriety of the § 103(a) rejection of claim 1.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Aaron Waxler, of NXP Corporation at (408) 474-9063 (or the undersigned).

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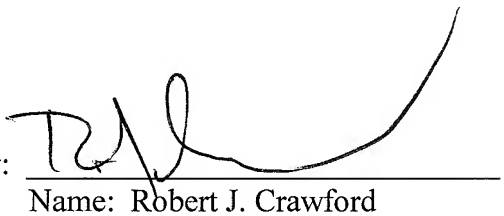
By: 

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